A Standardized Method for CMOS Unit Process Development

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Abstract—**A multi-purpose mask set, consisting of three stepper reticles, contains 95% of all test structures required for CMOS process development and random defect detection. Realizing the mask set by two dozen standard unit processes minimizes the feedback loop for defect density data, parametric data and unit process data.**

Introduction

Traditional mask sets for semiconductor process development typically consist of an assortment of parametric test structures and a VLSI circuit that passes through the complete manufacturing line prior to successful electrical testing [1]. As semiconductor manufacturing processes become longer and more complex, the feedback loop for information from VLSI circuits increases to unacceptable levels, and process engineers resort to an alternate method of data generation. Individual fabrication steps of a semiconductor process are grouped into short sequences of fabrication steps called unit processes, which are subsequently integrated into a full manufacturing process. Fabricating different unit processes in parallel using simple test structures provided by specialized unit process test mask sets reduces the feedback loop for parametric data, process margin data and confident defect density data from individual process levels [2], [3]. Since test structures on unit process test mask sets cannot identify multilevel defects, inspecting a VLSI circuit still constitutes the most effective method of identifying process failures of a more complex nature. However, complementary information from test structures on "short-loop" test mask sets assists in the development of manufacturing processes by tightly controlling unit processes.

Adding any new procedure to a manufacturing or research facility raises concern about its impact on day-to-day operations. For example, processing auxiliary test masks constitutes overhead activity, which could interfere with mainstream process development or manufacturing product wafers. Similar considerations apply to parametric testing, where additional wafers add to the normal work load. If separate patterns are used to fabricate each unit process, inventories of stepper reticles would increase dramatically, as would the number of test programs associated with these patterns. If, however, one standard unit process test mask set characterizes all levels of the overall process, the adverse effects of unit process development would be minimized.

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The Unit Process Control Mask Set

A recently developed unit process control mask set (UPCMS), consisting of a "lower" stepper reticle (LSR), a "holes" stepper reticle (HSR) and an "upper" stepper reticle (USR), includes virtually all structures required to examine conducting layers, inter-layer dielectrics, MOS transistors, photolithography, contacts and vias. The LSR contains all parametric structures and defect structures that analyze photolithography and conducting layers. The HSR contains all patterns that generate openings in any inter-layer dielectric, in addition to providing the bars for misalignment structures [14]. The USR contains all the patterns that examine inter-layer dielectrics in conjunction with patterns on the LSR and HSR. The LSR and USR can generate electrically testable patterns by themselves, which makes them useful for evaluating single conducting layers, as well as the conducting layers below and above inter-layer dielectrics. Features patterned by the LSR also provide topography for features patterned by the USR, while features patterned by both the LSR and the USR provide access to contact/via holes patterned by the HSR.

Multi-Purpose Structures

A brief literature search [1]–[6], [12]–[14] has yielded an extensive list of test structures required for the development of a complete CMOS process. Fabricating a multitude of realizations of the previously described Unit Process Control Mask Set can conceivably generate more than 95% of the structures on the list, and it allows a small set of multi-purpose structures, exhibited in Fig. 1, to analyze all failure modes of all CMOS unit processes. Fig. 2 indicates the location of these multi-purpose structures on a UPCMS stepper field.

Realization Through Standard Unit Processes [3]

A CMOS unit process can thus be defined as a sequence of manufacturing steps that can be realized with the UPCMS. About two dozen particularly useful UPCMS fabrication sequences commonly occur in the develop-

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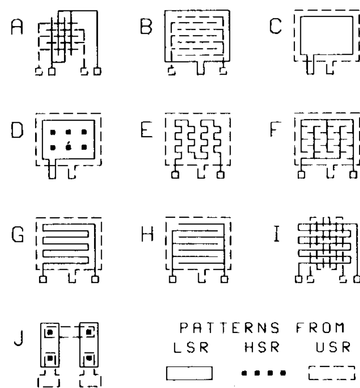

Fig. 1. Multi-purpose defect detection structures.

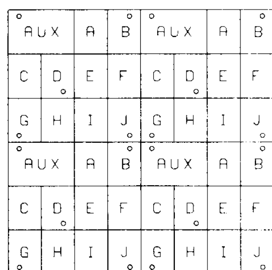

Fig. 2. Basic layout of UPCMS stepper field. The letters "A" through "J" denote the location of structures A through J in Fig. 1. The region labelled "AUX" contains auxiliary parametric structures. The circles depict the location of lithographic metrology cells. The stepping distance of the stepper field equals 14,570 micrometers in both the X- and Y-direction.

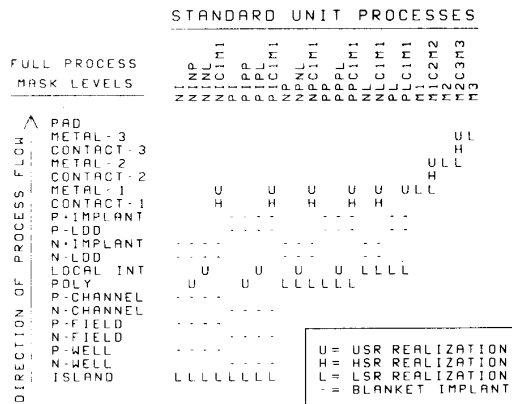

Fig. 3. A complex CMOS process is broken down into standard unit processes. The mask levels of the full process are listed on the left hand side of Fig. 3. Fabrication of the full CMOS process and associated standard unit processes proceeds in the direction of the arrow.

ment of most CMOS manufacturing processes, and are henceforth referred to as standard unit processes. Fig. 3 shows how each standard unit process analyzes a specific aspect of a complex CMOS manufacturing process that contains N+ polysilicon, P+ polysilicon, local interconnect and three levels of metal. The full process consists of 20 mask levels listed on the left side of Fig. 3. Fabrication proceeds in the direction of the arrow—from bottom to top. The right side of Fig. 3 exhibits the standard unit process realizations of the UPCMS, whose fabrication sequences also proceed from bottom to top.

Realizing standard unit processes on the UPCMS shortens their cycle time by eliminating a substantial number of fabrication steps. Blanket implants replace the masked implants of the full process, and UPCMS reticles cover the levels that exhibit critical geometries. For example, Standard Unit Process NINP includes blanket implants for the well, field, channel, LDD and N+ source/drain implants; the LSR patterns the island level; the USR patterns the poly/gate level. Descriptions of NINP and other standard unit processes follow in this section. Cross-sections resembling some of the standard unit processes are detailed in references [2] and [3].

Conducting Layers: Standard Unit Processes NP, PP, NL, PL, M1, M2 and M3 respectively characterize the N+ Polysilicon, P+ Polysilicon, N+ Local Interconnect, P+ Local Interconnect, Metal 1, Metal 2, and Metal 3 conducting layers. In each of these unit processes, the dielectric below the conducting layers mimics the dielectric below the conducting layers in the CMOS manufacturing processes, and thus is deposited, planarized and densified according to the prescribed procedures of the actual CMOS process. The respective conducting layers are subsequently deposited, possibly doped, patterned with the LSR, etched, possibly silicided, annealed and tested electrically, also according to the recipe of the CMOS manufacturing process. The structures generated by LSR patterns reveal the material properties and defect densities of the conducting layers. Applying a voltage between the structures and the substrate forms capacitors across the insulating dielectrics beneath the conducting layers.

Device Isolation: Standard Unit Processes NI and PI respectively explore isolation failure modes of NMOS and PMOS devices. The LSR generates island structures in P-doped substrate for NI and in N-doped substrate for PI. Blanket implants generate the correct dopant profile for isolation and conduction prior to silicidation, which is required for proper prober contact. Applying a voltage between the structures generated by Unit Processes NI and PI and the substrate forms diodes.

Gate and Field Devices: Standard Unit Processes NINP and PIPP characterize gate dielectrics, field oxides, gate capacitors, field capacitors, gate transistors and field transistors. For both unit processes the LSR acts as an island mask, which defines the isolation region and the active area. The gate dielectrics and polysilicon are deposited and doped according to the recipe of the CMOS manufacturing process, patterned with the USR and etched. Blanket implants provide the appropriate isolation doping. A high dose blanket source/drain implant of N-type dopant into P-substrate wafer completes the NMOS devices of Unit Process NINP, whereas a high

dose blanket source/drain implant of P-type dopant into N-substrate generates the PMOS devices of Unit Process PIPP. Devices can be tested electrically after silicidation. Sensitive transistors are placed near probe pads, in order to reduce series resistance.

Local Interconnect Devices: Standard Unit Processes NINL, PIPL, NPNL and PPPL respectively analyze the interfaces between conducting layers, such as N-island, P-island, N+ polysilicon or P+ polysilicon, and a local interconnect layer. The LSR patterns the lower conducting layers in the same manner as in Unit Processes NI, PI, NP and PP. The local interconnect layer is subsequently deposited, patterned by the USR, etched, possibly implanted and silicided. Spacer oxides need to be generated as prescribed by the recipe for the full CMOS process.

Interconnect Devices: Standard Unit Processes NIC1M1, PIC1M1, PLC1M1, NPC1M1, PPC1M1, NCC1M1, PLC1M1, M1C2M2 and M2C3M3 mimic the interconnect structures of the CMOS manufacturing process. Unit processes NI, PI, NP, PP, NL, PL, M1 and M2, patterned by the LSR, comprise the first mask levels of the interconnect unit processes, and they provide the lower conducting layers of interconnect structures. The appropriate inter-layer dielectric is subsequently deposited upon the patterned lower conducting layer, planarized, densified, patterned with the HSR, and etched to open contact holes. Finally, the appropriate upper conducting layer is deposited, patterned with the USR, and etched. In Unit Processes NIC1M1, PIC1M1, NPC1M1, PPC1M1, NLC1M1 and PLC1M1 the HSR patterns the Contact 1 level, and the USR defines Metal 1 features. Unit Process M1C2M2 evaluates the fabrication sequence Metal 1 → Contact 2 (Via 1) → Metal 2, while Unit Process M2C3M3 evaluates the fabrication sequence Metal 2 → Contact 3 (Via 2) → Metal 3.

Random Defect Detection [2], [6]

A comprehensive set of parametric test structures can make a critical contribution to the improvement of a CMOS process [1], but as the process defect density decreases, the yield of these structures increases until it approaches unity, and random defects become the dominant failure mechanism. Since the statistical significance of defect density measurements deteriorates rapidly for structure yields above 90% [7], stepper reticles typically contain insufficient area for a comprehensive set of confident parametric test structures. Only a VLSI circuit provides an estimate of defect density in a full CMOS process; thus the cycle time for defect density data equals the time required to manufacture and test VLSI circuits.

The UPCMS provides rapid defect density information by appropriately sizing the multi-purpose structures in Fig. 1. In order to detect random defects on all critical levels of a CMOS process, these structures must meet the following requirements.

Requirement 1: One four-inch wafer should provide enough area to measure a defect density with an expectation of 1 defect per square centimeter.

Requirement 2: The upper 95% confidence limit of a defect density measurement should not exceed the expectation by more than a factor of two.

Requirement 3: The UPCMS must detect defects in conducting layers, whose sheet resistances range from 0.02 ohms per square for pure aluminum, to 200 ohms per square for P+ source/drain implants.

Statistical confidence curves indicate that a broad range of selections for sample area and number of samples satisfies requirements 1 and 2 [7], but the ability to detect defects in a wide variety of conducting materials limits the maximum size of electrical test structures. For example, a parametric tester may find it difficult to measure the resistance of an extremely long and thin continuity structure, especially in a material with a high sheet resistance. Conversely, on wafers realized by Standard Unit Processes NI, PI, NINP, PIPP, NINL, PIPL, NIC1M1 and PIC1M1 reverse biased diodes insulate structures from the bulk of the wafer, and diode leakage can interfere with the detection of bridging defects by creating parasitic current paths. Examining the specifications of commercially available, automatic parametric test equipment and typical values for diode leakage indicates that a sample area of 0.033 square centimeters for all random defect detection structures fulfills all three of the previously listed requirements and frequently exceeds them. For example, the multi-purpose structures in Fig. 1 include a total of six large-area bridging structures. If the differences between these structures do not affect the outcome of an experiment, the number of available samples increases by a factor of six. In that case, the UPCMS can measure defect densities below 0.3 defects per square centimeter and still satisfy requirement 2 [7].

Successful random defect detection also depends upon the identification and elimination of systematic components of defect density. The UPCMS contains the following set of features, specifically designed for this purpose.

1) All structures intended for random defect detection have dual-probed pads, which check for proper probe contact.

2) Miniature versions of each random defect detection structure identify gross systematic failures related to that structure.

3) Fourfold repetition of identical structures on one reticle simplifies the detection of systematic and random reticle defects [8] and measures the effect of intra-chip parameter variations on defect density [9]. Fig. 4, for example, exhibits four instances of Structure B from Fig. 1, located at varying distances from the center of the stepper field. In stepper fields where stepper distortions increase as a function of distance from stepper field center, the yield of Structure B is much higher in Algebraic Quadrant 3 (Q3) than in Algebraic Quadrant 1 (Q1).

4) Since random defects follow the Poisson yield model

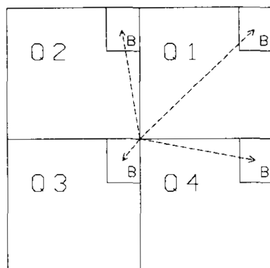

Fig. 4. Four-dice-per-stepper-field configuration. Arrows indicate the distance from the same point on each instance of Structure B to the stepper field center. Q1 through Q4 denote algebraic quadrants.

[10], comparing the yield from two structures, which are identical except for size, can identify systematic components of defect distributions [11]. For this reason, all structures of the UPCMS contain two substructures, one ten times as large as the other. The smaller substructure (area = 0.003 sq. cm.) also measures higher defect densities more confidently [7], which enhances its utility in the early phases of process development.

5) Auxiliary structures evaluate material properties such as sheet resistance [12], lithographic parameters, process margins and reliability issues such as electromigration [13].

Comprehensive Analysis of Photolithography

A wide variety of structures on the UPCMS permits photolithography engineers to address most patterning issues. Four instances per stepper field of the LSR features of Structures A, E, F, G, H and I from Fig. 1 confidently determine the random defect density of the patterning process. Each auxiliary region of the UPCMS (AUX in Fig. 2) includes electrically testable structures that evaluate anisotropy, reticle bias and proximity effects. Fig. 2 also indicates the location of 20 lithographic metrology cells that contain electrically testable linewidth structures and misalignment structures [14] for both the X-direction and Y-direction. (The HSR provides the slots for misalignment structures; the LSR provides most lithographic features.) These cells also include critical dimension bars and box-in-box structures for electron microscopy based metrology.

The large number of measurement sites on the UPCMS suffices to draw a comprehensive map of intra-chip parameter variations, which enables photolithography engineers to characterize wafer steppers, resist processes and mix-and-match processes between a variety of lithography tools. Fig. 5, for example, exhibits misalignment data for a mix-and-match process between a wafer stepper and an electron beam direct write machine. Each vector represents the mean misalignment measured by electrical misalignment structures on 100 lithographic metrology cells from 100 different stepper fields on five wafers. The mean translation vector has been subtracted off.

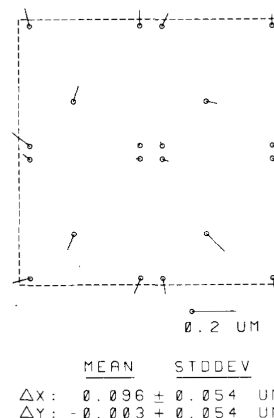

Fig. 5. Die map of misalignment data from lithographic metrology cells. X and Y represent the mean translation vector, which has been subtracted off.

Design Rule Optimization and Process Margin Analysis

Each UPCMS reticle is customized to one specific nominal set of design rules exhibited by all geometry-dependent random defect detection structures. The UPCMS also includes five instances of every multi-purpose structure in Fig. 1 that contain geometry-dependent components. These structures, all exhibiting the same pitch, are repeated at biases ranging from 0.2 micrometers thicker than nominal to 0.2 micrometers thinner than nominal, in 0.1 μm increments. Any failures of the structures result from systematic process problems, because they are too small (Area ~ 0.0001 square centimeters) to capture random defects [7]. The variably biased structures can thus be used effectively to determine the optimal patterning conditions and process margins of a specific standard unit process. For example, frequent failures of bridging structures exhibiting thick lines and narrow gaps indicate that nominal bias generates oversized features, whereas frequent continuity failures of structures exhibiting thin lines and wide gaps indicate that nominal bias generates undersized features. Changing the nominal bias or exposure parameters can correct either problem, but frequent failures of both types of structures indicate a narrow and potentially unstable operating range for the specific unit process at nominal pitch. Such insufficient process latitude may require a relaxation of design rules, which are subsequently analyzed by a UPCMS that reflects the new design rules.

Unit Process Identification

Including the structures in Fig. 6 on the UPCMS permits a parametric tester to differentiate between standard

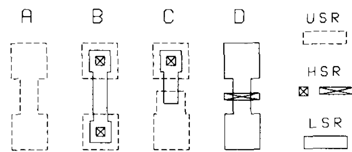

Fig. 6. Structures for standard unit process identification. A voltage is applied from the top end to the bottom end of each structure.

unit processes. An electrical short in Structure A identifies the existence of an upper conducting layer. An electrical open identifies standard unit processes with only a single conducting layer patterned by the LSR. A short in Structures A and B detects the presence of USR and HSR features that characterize 3-level, interconnect-oriented standard unit processes. A short in Structure A and an open in Structure B detect Standard Unit Processes NINP and PIPP, which form gate and field devices. A short in Structure C identifies standard unit processes such as NINL, PIPL, NPNL and PPPL, whose upper conducting layer is local interconnect. An open in Structures A and D identifies a lithographic misalignment test such as the one in Fig. 5.

Applying positive and negative voltages from the lower conducting layer to the wafer chuck specifies the nature of the lower conducting layer. Yielding an open circuit in both cases implies that the lower conducting layer rests on an insulator. An open circuit for the positive voltage and a short circuit for a negative voltage indicate the lower conducting layer is an N+ implant in a P-substrate, whereas the converse refers to a P^+ implant in an N-substrate. A sheet resistance measurement separates the various types of conducting layers that rest on insulators from each other, and completes the identification of the standard unit process. [3]

Standard Tests

An analogous set of tests and data analysis routines is associated with each standard unit process. A basic test checks for prober contact, identifies the standard unit process, and evaluates the fundamentals of conducting layers and dielectrics. A bias/margin test evaluates the variably-biased miniature and auxiliary structures. Selecting the die configuration in Fig. 7 for the bias/margin test enables process engineers to characterize process margins with minimal tester time, by promoting statistically designed experiments. The strategic location of the eight dice characterizes both intra-stepper-field and inter-stepper-field parameter variations. Die maps such as the one in Fig. 5 typically display intra-stepper-field parameter variations; numeric wafer maps generally convey inter-stepper-field parameter variations.

A random defect test evaluates all pertinent large area structures on all dice, in order to determine random defect density with statistical significance [7]. Fig. 8 shows the results of a random defect test for a bridging structure on a UPCMS wafer from a lot realized by a photolithography-oriented unit process [15]. Data analysis routines [16] were able to separate true random defects from wafer-edge-induced failures and reticle-induced repeat defects, which occurred at the same locations on all wafers of the lot [2].

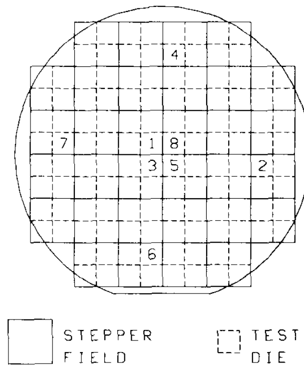

Fig. 7. Wafer map depicting die selection sequence of bias/margin test. Prober visits dice in ascending numerical order.

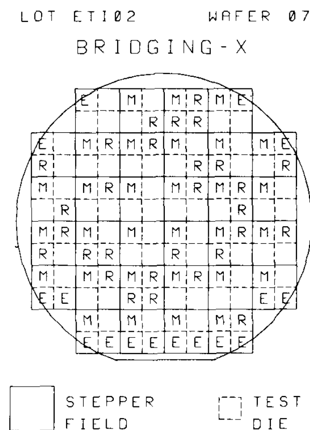

Fig. 8. Wafer map of UPCMS yield data for bridging device from Structure G of Fig. 1. A letter indicates that the device at that specific location has failed. The letters "E", "M" and "R" respectively denote wafer-edge-induced failures, mask-induced repeat defects and apparent random defects.

Applications

UPCMS applications evolve with the development of a CMOS manufacturing process, typically in the five steps outlined below. Since the UPCMS design can be customized for any set of design rules, these steps repeat with the development of successive CMOS processes. The same test software can evaluate all UPCMS customizations [2].

1) Prior to any UPCMS implementation, a device/lithography oriented mask set is realized by key standard unit processes. The wide range of geometries exhibited

by the test structures on this mask set permit design engineers to establish targets and ranges for the design rules of each mask level. A target is typically set at a value where devices that deviate from the target by 25% in either direction still yield.

2) A USR, HSR and LSR, whose design rules fall within the $\pm 25\%$ range of every critical process level, is fabricated and realized in parallel by all standard unit processes. This initial set of experiments determines the optimal lithography and process bias for every mask level, and compares defect density from level to level. The conducting layer material with the lowest defect density is typically chosen for lithography control [15].

3) For about 20% of the standard unit processes, the optimal bias of a process level deviates significantly from the nominal bias of the initial UPCMS reticles, and additional reticles need to be generated. The enhanced reticle set becomes a vehicle for unit process control, because it provides rapid feedback on parametric data, process margin data, defect density data and information pertinent to process integration. Improving the full process will, in turn, result in modifications of the standard unit processes.

4) When the yield of the variably biased miniature structures for a specific standard unit process approaches 100%, the large area defect detection structures on the UPCMS typically indicate a defect density of 1 to 4 defects per square centimeter with 95% confidence [7]. Once the upper 95% confidence limit of defect density data for all standard unit processes drops below 2 defects per square centimeter, the expectation for defect density of the full CMOS process approaches 1 defect per square centimeter. At that point in time, manufacturing facilities begin to exercise key standard unit processes with an identical copy of the UPCMS, in order to prepare for an orderly transfer of the full CMOS process.

5) In manufacturing, the UPCMS serves as a yield improvement vehicle until the defect density of standard unit processes reaches one defect per square centimeter. Then specialized test mask sets, which contain very large area versions of one of the structure types from Fig. 1, drive the defect density of unit processes down to the 0.1 defect per square centimeter range, and the UPCMS is used for trouble shooting only.

Results

The UPCMS has become the most commonly used mask set at Hewlett-Packard Corporation's Integrated Circuit R&D Center: about 40% of all wafers emerging from the wafer fabrication facility exhibit UPCMS patterns. The majority of process development engineers have utilizied the UPCMS as a vehicle for stepper characterization, lithography control, gate oxide integrity checks, FET characterization, interconnect development, defect reduction on all process levels or process margin analysis. Unit process development activities are converging towards routine execution of the standardized unit process formats, and the standardized tests provide process engineers with pertinent data in a timely manner. The comprehensive nature of the UPCMS has permitted it to replace all other CMOS unit process test mask sets, which has dramatically reduced the stepper reticle inventory and the frequency of reticle changes. Since the UPCMS only contains one probe pad pattern, probe card changes at the tester have also become a rare event. All these factors increase the stepper's availability for processing wafers or the parametric tester's availability to evaluate wafers, which contributes substantially to the reduction of overhead activities, both at the R&D center and at manufacturing facilities.

Hewlett-Packard has given a copy of the UPCMS to Sematech, which uses it as a vehicle for defect reduction and equipment evaluation. Sematech has made the UPCMS design available to member companies and select universities through the Centers of Excellence program.

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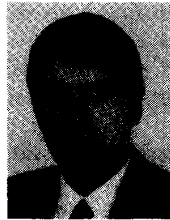

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In 1982 he joined the Hewlett-Packard Corporation as a Process Engineer in an integrated circuit manufacturing facility, where he developed his research interest in the productivity of manufacturing systems. In 1985 he became a member of the technical staff of HP's Integrated Circuit Research and Development Center, working primarily in the field of microelectronic test structures. In 1989 he designed a series of productivity-oriented test chips for HP and Sematech, including short-loop monitors for process control, defect reduction and improved manufacturability.